REMARKS

Claims 1 to 23 are pending in this application of which claims 1, 7, 10 and 17 are the independent claims. Favorable reconsideration and further examination are respectfully requested.

Claims 1-4, 7 and 9 were rejected under 35 U.S.C. § 102(b) over Bolam (Patent Application Publication No. 2002/0043686); claims 5, 6, 8, 10 to 15 and 17 to 22 were rejected under §103 over Bolam; and claims 16 and 23 were rejected under § 103 over Bolam in view of Lee (U.S. Patent No. 6,251,782). As shown above, Applicants have amended the claims to define the invention more clearly. In view of these amendments, withdrawal of the art rejections is respectfully requested.

Claim 1, as amended, is directed to a tiedown structure. The tiedown structure includes a semiconductor substrate that has a chip formed thereon. The chip includes an electrical device. The structure also includes a kerf region proximate the chip and a conductive connector that forms an electrical connection between the chip and the kerf region. The device is grounded by the conductive connector to prevent charge overloading of the device during a processing step.

The applied art is not understood to disclose or suggest the foregoing features of claim 1. In particular, Bolam does not disclose or suggest that "the device is grounded by the conductive connector to prevent charge overloading of the device during a processing step."

Specifically, the diffusion protection layer 202 does not ground the transistor to prevent charge overloading. Instead, diffusion protection layer 202 prevents diffusion of mobile ions

such as sodium ions or other positive ion contaminants, into the sidewalls of recess 204 (see FIG. 7A of Bolam) and into the remaining portions of oxide layer 212', 212 of the SOI substrate.

Moreover, FIG. 7B of Bolam shows that there is no electrical connection between the sidewall protection layer 212 and any transistor because layer 212 is electrically insulated from other devices by a gate oxide deposited on layer 214' and by an upper insulating layer portion. Transistors are disposed in any region of an integrated circuit but not at the outer edge of the integrated circuit. Accordingly, a conductive line from the outer edge of the integrated circuit to the transistor would be required as illustrated in FIG. 6 of Applicants' specification to ground the transistor. For example, in FIG. 6 of Applicants' specification, the conductive layer 54 connects the outer edge 12 of the circuit with transistor 20, which lies well within the integrated circuit. In contrast, diffusion protection layer 202 of Bolam only reaches to an insulating dielectric portion adjacent to an outer contact within layer 214'; and therefore, any electrical connection by the diffusion protection layer to the transistor or to a transistor electrode is nonexistent.

Since Bolam does not disclose or suggest that the device is grounded by the conductive connector to prevent charge overloading of the device during a processing step, claim 1 is believed to be patentable over Bolam.

Claim 7, as amended, is directed to a tiedown structure. The structure includes a semiconductor substrate that has a chip formed thereon. The chip includes an electrical device. The tiedown structure also includes an edge seal along an outer perimeter of the chip and a conductive connector that forms an electrical connection between the edge seal and the device to ground the device and to prevent charge overloading of the device during a processing step.

The applied art is not understood to disclose or suggest the foregoing features of claim 1. In particular, Bolam does not disclose or suggest "a conductive connector forming an electrical connection between the edge seal and the device to ground the device and to prevent charge overloading of the device during a processing step."

Specifically, Bolam does not use its diffusion protection layer 202 to ground the transistor as in claim 1. Since Bolam does not disclose a conductive connector forming an electrical connection between the edge seal and the device to ground the device and to prevent charge overloading of the device during a processing step, claim 7 is believed to be patentable over Bolam.

Claim 10, as amended, is directed to a method for forming a semiconductor structure. The method includes forming a device on a chip, defining a kerf proximate the chip, and forming an electrically conductive connector. The conductive connector connects the device and the kerf for grounding the device during a subsequent processing step. The method also includes completing fabrication of the chip including performing the processing step, and removing an end of the conductive connector from the kerf thereby preventing short circuits to ground of the device during device operation.

The applied art is not understood to disclose or suggest the foregoing features of claim 10. In particular, Bolam does not disclose or suggest "the conductive connector connecting the device and the kerf for grounding the device during a subsequent processing step."

Specifically, Bolam does not use its diffusion protection layer 202 to ground the transistor as discussed above for claim 1. Since Bolam does not disclose or suggest the conductive connector connecting the device and the kerf for grounding the device during a subsequent processing step, claim 10 is believed to be patentable over Bolam.

Claim 17, as amended, is directed to a method of forming a semiconductor structure. The method includes forming a chip on a semiconductor substrate, the chip including a device, forming an edge seal along an outer perimeter of the chip and forming an electrically conductive connector. The conductive connector connects the edge seal and the device for grounding the device during a processing step. The method further includes completing fabrication of the chip, which includes performing the processing step, and removing a portion of the conductive connector thereby preventing short circuits to ground during device operation.

The applied art is not understood to disclose or suggest the foregoing features of claim 17. In particular, Bolam does not disclose or suggest "the conductive connector connecting the edge seal and the device for grounding the device during a processing step." Specifically, Bolam does not use the diffusion protection layer 202 to ground the transistor as in claim 1.

Since Bolam does not disclose or suggest the conductive connector connecting the edge seal and the device for grounding the device during a processing step, claim 17 is believed to be patentable over Bolam.

Lee, which was cited solely for its disclosure of ion beam milling, is not understood to add anything that would remedy the foregoing deficiencies of Bolam vis-à-vis the claims. Accordingly, Applicants submit that the entire application is now in condition for allowance. Such action is respectfully requested at the Examiner's earliest convenience.

All correspondence should be directed to the below address. Applicants' attorney can be reached by telephone at the number shown below.

No fee is believed to be due for this Response; however, if any fees are due, please apply such fees to Deposit Account No. 06-1050 referencing Attorney Docket 13292-009001.

Respectfully submitted,

Date: August 6, 2003

Paul A. Pysher
Reg. No. 40,780

Fish & Richardson P.C.
225 Franklin Street
Boston, Massachusetts 02110-2804
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

20700793.doc